FORM PTO		U.S. Department ent and Trademark		Attorney Docket Number , 5646-114		Serial No. To Be Assigned				
LIST	OF D	OCUMENTS CITE	ED BY APPLI							
	(L	lse several sheets if	necessary)			-	10/663,624			
				Applicants: Paul Murtagh						
					Filing Date: Concurrently Herewith			Group 28/6		
U. S. PATENTS & PATENT APPLICATION PUBLICATIONS										
Examiner Initial		Document Number	Date	N	ame	Class	Subclass	Filing Date if Appropriate		
und	1	6,593,786	7/15/03	Jung		327	158			
und	2	6,586,978	7/1/03	Stief		327	158			
und	3	6,584,578	6/24/03	Faue		713	503			
und	4	6,584,021	6/24/03	Heyne et al.		365	194			
. Und	5	6,539,072	3/25/03	Donnelly et al		375	371			
hi	6	6,518,807	2/11/03	Cho		327	158			
und.	7	6,504,408	1/7/03	von Kaenel		327	158			
w/	8	6,501,328	12/31/02	Gauthier et al.		327	551			
my	9	6,501,312	12/31/02	Nguyen		327	161			
ind,	10	6,295,328	9/25/01	Kim et al.		375	376			
unt	11	2003/0154447	8/14/03	Gauthier et al.		716	2			
und	12	2003/0154417	8/14/03	Drexler		713	400			
ind	13	2003/0151433	8/14/03	Takai		327	158	-		
(WH	14	2003/0141910	7/31/03	Reindl		327	158			
in	15	2003/0117194	6/26/03	Lee		327	158			
land	16	2003/0117193	6/26/03	Lee		327	158			
ind	17	2003/0108139	6/12/03	Jung		375	376			
La!	18	2003/0099321	5/29/03	Juan et al.		375	376			
ind	19	2003/0095009	5/22/03	Gomm et al.		331	57			
in/	20	2003/0094984	5/22/03	Weis et al.		327	182			
und	21	2003/0090296	5/15/03	Yoo		327	12			
w	22	2003/0071668	4/17/03	Starr		327	157			
in	23	2003/0067335	4/10/03	von Kaenel		327	158			
<u>1044</u>	24	2003/0058014	3/27/03	Krishnamurty		327	158			
m	25	2003/0052719	3/20/03	Na		327	158			

**EXAMINER** \*EXAMINER

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	Pat OF D	U.S. Department of Commerce ent and Trademark Office  OCUMENTS CITED BY APPLICANT  Jse several sheets if necessary)	Attorney Docket Number 5646-114	Serial No. To Be Assigned			
			Applicants: Paul Murtagh				
	_		Filing Date: Concurrently Herewith	Group 28/6			
		OTHER DOCUMENTS (Including Author	or, Title, Date, Pertinent Pages, Etc.)				
h	26	Moon et al., "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance," IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000					

EXAMINER 2 \*EXAMINER

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\*EXAMINER

**EXAMINER** 

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